REMARKS

Claims 1, 4-7, 10-13, 15, 18, 21-23, and 25-27 are pending. Claims 1, 7, 15, and 18 are in independent form.

In the action mailed August 10, 2006, claim 7 was objected to as allegedly reciting limitations out of order. Although claim 7 has been amended to address the Examiner's concerns, this has been done to improve the readability of the claim and does not imply that these limitations need be performed in the recited order. Instead, Applicant submits that it is improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order. *See, e.g., M.P.E.P.* § 2111.01 (*citing Altiris Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371 (Fed. Cir. 2003)).

CLAIM 1

Claim 1 has been amended to recite subject matter drawn from former claim 3. Former claim 3 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent Publication No. 2002/0023250 to Yumoto et al. (hereinafter "Yumoto"), the publication entitled "A multi-representational design data

capture system," by K. Yamagishi (hereinafter "Yamagishi"), and the publication entitled "IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language" (hereinafter "IEEE Std. 1364-1995").

As amended, claim 1 relates to a system that includes a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit, wherein the logic design includes labels and a central database integrated with the logic design module and including a collection of modifiable values of signal parameters that are accessible by the logic design module, where the values of signal parameters are associated with the labels in the logic design.

The logic design module is operable to update the logic design to reflect modification of the values of the signal parameters in the central database by modifying the logic design to be compatible with the modified values of the signal parameters, and to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically.

The rejection contends that it would have been obvious for one of ordinary skill to combine Yumoto, Yamagishi, and the IEEE Std. 1364-1995 to arrive at a logic design module that is operable to update the logic design and to indicate design discrepancies in the logic design, as recited in claim 1. Applicant respectfully disagrees.

In this regard, Yumoto describes a parameterized method for designing data driven media processors (DDMP). *See, e.g., Yumoto*, Title. FIGS. 5-12 of Yumoto illustrate the various hierarchical levels of a DDMP. *See, e.g., Yumoto*, paras. [0038]-[0045]. Elements at these various hierarchical levels of a DDMP can be changed by a user selection of a predefined set of values for a collection of parameters. *See, e.g., Yumoto*, para. [0090]-[0092] (describing that three different "value units," each of which includes a variety of associated values, can be selected by a user); para. [0085] (describing that the data width bit and number of parallel data stored in a memory unit are "preset"). *See also Yumoto*, FIG. 13 (showing predefined parameter values for the "min condition," the "typ condition," and the "max condition"); para. [0087] (describing that the elements required to design other functional blocks are

"extracted in advance" and parameterized); para. [0089] (describing that Yumoto's parameterize RTL design tool automatically produces an RTL descriptor file based on such "predetermined parameters").

Such predetermined sets of values can be selected for "each functional block" of a DDMP. *See, e.g., Yumoto*, para. [0101]-[0103]. Examples of prototype library files of such functional blocks are shown in Yumoto's FIGS. 15-17. *See, e.g., Yumoto*, para. [0048]-[0050]; [0093]. Such prototype library files are used with a predetermined sets of values to produce RTL descriptions as shown in FIGS. 18-20. *See, e.g., Yumoto*, para. [0093]; [0051]-[0053]; [0094]. As best understood by applicant, the inputs or outputs of the functional blocks are not changed through the user selection of different predetermined sets of values. *See, e.g., Yumoto*, FIGS. 18-20.

Against this backdrop, the rejection contends that it would have been obvious to add IEEE Std. 1364-1995's comparison between bit lengths of port expressions in instance arrays and bit lengths in single instance ports so that Yumoto's parameterized method could indicate design discrepancies in a logic design. Applicant respectfully disagrees.

To begin with, Applicant is at a loss to understand how the comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports in IEEE Std. 1364-1995 indicate design discrepancies. To the best of applicants' understanding, the IEEE Std. 1364-1995 comparison *determines* how single instance ports/terminals in an instantiated module are to be connected to ports/terminals in an instance-array port expression. *See IEEE Std. 1364-1995*, page 59, line 5-9. In other words, the IEEE Std. 1364-1995 comparison appears to be part of the *generation* of a logic design, rather than an indication of design discrepancies in a logic design, as recited in claim 1.

Moreover, as discussed above, Yumoto's users select a predefined set of values for a collection of parameters for "each functional block" of a DDMP. It would seem unlikely that such predefined set of values could potentially have internal design discrepancies of the type that would require checking. Rather, it would appear likely that the predefined sets of values for each functional block would be defined to be internally consistent, i.e., without design discrepancies. No design discrepancies in the logic design would be likely to result from the user selection of such an internally consistent set of values. Accordingly, applicant submits that it would not

be obvious for one of ordinary skill to add the IEEE Std. 1364-1995 comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports to check the consistency of Yumoto's functional blocks.

For these reasons, applicant submits that claim 1 is not obvious over the combination of Yumoto, Yamagishi, and IEEE Std. 1364-1995. Accordingly, applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 7

Claim 7 has been amended to recite subject matter drawn from former claim 9. Former claim 9 was rejected under 35 U.S.C. § 103(a) as obvious over Yumoto, Yamagishi, and IEEE Std. 1364-1995.

As amended, claim 7 relates to a method that includes receiving an assignment of a value to a signal parameter, maintaining the value of the signal parameter in a central database in association with an identifier of the signal parameter, using the identifier of the signal parameter maintained in the central database to identify a first position in computer code for a logic design forming part of an electrical circuit, modifying the computer code at the first position to reflect the value, using the identifier of the signal parameter maintained in the central database to identify

a second position in the computer code for the logic design, modifying the computer code at the second position to reflect the value, receiving an updated value of the signal parameter in the central database, updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter, and indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

The rejection contends that it would have been obvious for one of ordinary skill to combine Yumoto, Yamagishi, and the IEEE Std. 1364-1995 to indicate design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter, as recited in claim 7. Applicant respectfully disagrees.

In this regard, as discussed above, Yumoto's parameterized method uses predefined sets of values for a collection of parameters to change elements for each functional block of a DDMP. The inputs or outputs of such functional blocks do not appear to be changed through the user selections. It would seem unlikely that such predefined set of values could potentially have internal design discrepancies of the type that would require checking to indicate design discrepancies, as recited in claim 7.

Moreover, it is not clear to application that IEEE Std. 1364-1995's comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports so indicate design discrepancies. To the best of applicant's understanding, the IEEE Std. 1364-1995 comparison *determines* how single instance ports/terminals in an instantiated module are to be connected to ports/terminals in an instance-array port expression as part of the *generation* of a logic design, rather than an indication of design discrepancies in a logic design, as recited in claim 7.

For these reasons, applicant submits that claim 7 is not obvious over the combination of Yumoto, Yamagishi, and IEEE Std. 1364-1995. Accordingly, applicant requests that the rejections of claim 7 and the claims dependent therefrom be withdrawn.

CLAIM 18

Claim 18 has been amended to recite subject matter drawn from former claim 20. Former claim 20 was rejected under 35 U.S.C. § 103(a) as obvious over Yumoto, Yamagishi, and IEEE Std. 1364-1995.

As amended, claim 18 relates to a machine-accessible medium containing instructions which cause a machine to perform operations. The operations include receiving a value of a signal parameter that characterizes multiple bits of a multiple

bit signal, maintaining the value of the signal parameter in a central database, using the value of the signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal, receiving an update to the value of the signal parameter in the central database, updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated signal parameter, and indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

The rejection contends that it would have been obvious for one of ordinary skill to combine Yumoto, Yamagishi, and the IEEE Std. 1364-1995 to indicate design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter, as recited in claim 18. Applicant respectfully disagrees.

In this regard, as discussed above, Yumoto's parameterized method uses predefined sets of values for a collection of parameters to change elements for each functional block of a DDMP. The inputs or outputs of such functional blocks do not appear to be changed through the user selections. It would seem

unlikely that such predefined set of values could potentially have internal design discrepancies of the type that would require checking to indicate design discrepancies, as recited in claim 18.

Moreover, it is not clear to application that IEEE Std. 1364-1995's comparisons between bit lengths of port expressions in instance arrays and bit lengths in single instance ports so indicate design discrepancies. To the best of applicants understanding, the IEEE Std. 1364-1995 comparison determines how single instance ports/terminals in an instantiated module are to be connected to ports/terminals in an instance-array port expression as part of the generation of a logic design, rather than an indication of design discrepancies in a logic design, as recited in claim 18.

For these reasons, applicant submits that claim 18 is not obvious over the combination of Yumoto, Yamagishi, and IEEE Std. 1364-1995. Accordingly, applicant requests that the rejections of claim 18 and the claims dependent therefrom be withdrawn.

CLAIM 15

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Yumoto and Yamagishi.

As amended, claim 15 relates to an apparatus that includes a central database accessible by one or more users, modification logic to allow a user to modify the values associated with the identifiers individually, and an interface to convey the identifiers and the associated values from the central database to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit. The central database includes a collection of identifiers of one or more bit width signal parameters and values associated with each of the identifiers of the bit width signal parameters.

As discussed above, Yumoto's parameterized method uses predefined sets of values for a collection of parameters to change elements for each functional block of a DDMP. Yumoto does not allow a user to modify values associated with the identifiers individually. Rather, multiple values are always modified as a set.

Yamagishi does nothing to remedy this deficiency in Yumoto. Indeed, Yamagishi has nothing to do with modification logic to allow a user to modify the values associated with identifiers.

Accordingly, applicant submits that claim 15 is not obvious over the combination of Yumoto and Yamagishi. Applicant therefore requests that the rejection of claim 15 be withdrawn.

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Scott C. Harris
Reg. No. 32,030

BY
JOHN F. CONROY
REG. NO. 45,485

Fish & Richardson P.C.
PTO Customer No. 20985
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

SCH/JFC/jhg
10678114.doc